REMARKS:

1) Referring to item 12) of the Office Action Summary, the Examiner is respectfully requested to acknowledge receipt of the foreign Priority Document, which was filed herein on April 15, 2003 and received in the USPTO on April 21, 2003, as proven by our return receipt postcard, a copy of which is enclosed.

2) The only amendments being made involve the revision of the Title of the Invention to be more descriptive, and correction of a typographical error at line 17 of claim 21. These amendments do not introduce any new matter. Entry thereof is respectfully requested.

3) Referring to section 2 on page 2 of the Office Action, the Title of the Invention has been revised to be more clearly descriptive of the invention as claimed. Withdrawal of the objection to the Title is respectfully requested.

4) Referring to section 7 on page 5 of the Office Action, the indication of allowable subject matter in claims 24, 26 to 28, 31, 32, 35 and 36 is appreciated. These claims have been maintained without amendment, so they should still be seen as containing the indicated allowable subject matter. Furthermore, for the reasons that will be discussed below, it is respectfully submitted that independent claim 21 is itself patentable over the prior art of record, so that the claims with indicated allowable subject matter are maintained as dependent claims.

5) Referring to section 5 on pages 2 to 4 of the Office Action, the rejection of claims "21-23 and 25" as obvious over US Patent 6,160,413 (Habersetzer et al.) in view of US Patent 6,046,947 (Chai et al.) is respectfully traversed. From the further detailed discussion of this rejection, it appears that the rejection also applies to claims 29, 30, 33 and 34.

6) Present independent claim 21 is directed to a method of testing an integrated circuit, comprising certain specified steps.

Step a) defines at least one "signal output pin" by reciting that an output signal generated by a circuit unit of the integrated circuit is provided to such "signal output pin" during a normal operating mode".

Step b) involves externally applying a potential to at least one selected **output** pin among the signal output pin or pins of the IC. This is a very significant feature of the invention. As will be discussed next, this potential that is externally applied to a signal **output** pin will trigger the IC to switch from a normal operating mode into a test mode. The prior art does not disclose and would not have suggested such a step or feature of externally applying a potential to a signal output pin so as to cause an IC to switch from a normal operating mode into a test mode dependent on and responsive to the externally applied potential.

Steps c) and d) of present claim 21 involve evaluating the potential value of the externally applied potential, and

switching from the normal operating mode into the test mode dependent on and responsive to a result of this evaluating.

Step e) of the claim involves generating a test signal during the test mode and providing the test signal to at least one of the signal output pin or pins.

So, in the inventive method, it is significant that a normal operating output signal is provided to one or more signal output pins during the normal operating mode, an external potential is applied to at least one of the signal output pins to switch the IC into a test mode, and then a test signal generated during the test mode is provided to at least one of the signal output pins. In other words, the normal operating output signal as well as the test signal are respectively **outputted** from one or more signal **output** pins, and the testing trigger potential is externally applied as an **input** to at least one of the signal **output** pins.

7) As acknowledged by the Examiner, Habersetzer et al. **do not disclose** externally applying a potential to at least one selected **output** pin to thereby trigger the IC to switch from a normal operating mode into a test mode.

In fact, all of the teachings of Habersetzer et al. are clearly and significantly to the contrary.

According to Habersetzer et al., an integrated circuit arrangement includes normal operating circuitry (12) and test circuitry (14) that are connected to each other and that are each connected to a set of input pins (16) and a set of output pins (18) (see Fig. 1 and col. 3, lines 50 to 67). During normal operation, input signals are provided via the input pins (16) to

the normal operating circuitry (12), which then generates output signals provided to the output pins (18) (col. 3, lines 52 to 55). So, the output pins (18) could be said to correspond in this regard to the at least one signal output pin defined in step a) of present claim 21.

Furthermore, during a test mode according to Habersetzer et al., input signals are received by the test circuitry (14) via the **input** pins (16), whereby these input signals may be test vectors which may also be received by the normal operating circuitry (col. 3, lines 55 to 57). The test circuitry may also receive control signals from the operational circuitry during a test mode (col. 3, lines 58 to 62). Then, test result data is output via the output pins (18) (col. 3, lines 63 to 64).

It is thus clear from the disclosure of Habersetzer et al., that external potentials are **not** applied to the output pins (18), but rather to the **input** pins (16). In further detail, the "test vectors", "test input signals", or particularly "test key select inputs" are provided to a "test mode latching circuit" (20) of the test circuitry (14) in order to select and trigger the particular intended test mode (see col. 1, lines 56 to 60; col. 4, lines 1 to 8 and 38 to 43; col. 9, lines 19 to 26; etc.).

From these express disclosures of Habersetzer et al., a person of ordinary skill in the art would have expected and understood only that test trigger signals (e.g. test key select inputs) should be provided to the test circuitry only via the **input** pins (16), either directly to the test circuitry (14), which includes the test-mode latching circuit (20) incorporated therein, or via the operational circuitry (12) which also

receives its inputs from the input pins (16). A person of ordinary skill in the art would have had **NO** motivation or suggestion toward externally applying a potential to one of the **output** pins (18), because those output pins according to Habersetzer et al. serve only for outputting result signals. From the reference, a person of ordinary skill in the art would have had no idea whatsoever regarding the significantly different concept according to the invention.

8) The Examiner has referred to Chai et al. for allegedly disclosing a method of testing an integrated circuit involving a step of "*externally applying an externally applied potential (Vdd) ... to at least one selected one-signal output pin (output driver 14)*". This assertion is respectfully traversed as factually incorrect.

Chai et al. disclose an integrated circuit memory arrangement and method for testing the same. The arrangement includes a plurality of cascaded memory blocks or memory arrays (10, 20) that are pipelined together through latch units (12, 22), and respectively connected to output pins (DQ1, DQ2) through output drivers (14, 24). In normal operation, data is provided from the memory arrays (10, 12) through the latch units to the output drives (14, 24) (col. 3, lines 33 to 52). So, the output drives (14, 24) might be compared to the at least one signal output pin as defined in step a) of present claim 21.

The arrangement further includes a test mode control circuit (30) which can switch the arrangement from the normal operating mode into a test mode (col. 3, lines 53 to 60). The test mode

control circuit (30) is triggered to switch from the normal operating mode into the test mode, in response to an externally applied test mode control signal ΦDAE that is **externally applied to a special test mode control signal input pin** of the control circuit (30) (see col. 3, lines 62 to 64; col. 4, lines 50 to 55; etc.; as well as the top middle portion of the test mode control circuit (30) near the middle of Fig. 1 and the middle of Fig. 2). When switched to the test mode, the control circuit (30) will pass data serially from one pipelined latch unit to the next (col. 4, lines 52 to 65; col. 6, lines 48 to 54; etc.). The further processing of data during the test mode is controlled by a test clock signal (TCLK) and a test read signal (ΦTRL), which are also externally applied to special test signal input pins of the latch units (12, 22) (see col. 2, lines 22 to 47; col. 4, lines 14 to 45; etc.).

Thus, it is absolutely clear from the disclosure of Chai et al., that the potentials externally applied to the circuit for triggering the test mode include the externally applied signals ΦDAE, ΦTRL, and TCLK, which are all respectively applied to special test signal **input** pins on the test mode control circuit (30) and on the latch units (12, 22). There is **NO** disclosure or suggestion toward applying any one of the signals ΦDAE, ΦTRL or TCLK, or any other test-triggering signal to the **output** pins (DQ1, DQ2, 14, 24).

It is further not seen how the Examiner is asserting that the externally applied potential (Vdd) is applied to the output driver (14), because actually the voltage (Vdd) is applied to a transistor within the test mode control circuit (30) (see Fig.

1 and col. 2, lines 18 to 22). That terminal of the transistor receiving the voltage (Vdd) is not a signal output pin. Also, that voltage (Vdd) is not evaluated so as to cause the circuit to switch from the normal operating mode into a test mode responsive to and dependent on the result of such evaluation. To the contrary, the reference makes absolutely clear that switching from the normal mode to the test mode is triggered in response to the test control signal (ϕDAE) applied to the special external test signal input pin for this purpose.

9) For the above reasons, even a combined reading of the two references by a person of ordinary skill in the art, would have given no suggestion or motivation whatsoever toward the presently claimed method, which requires externally applying a potential to a signal output pin, then evaluating this externally applied potential and switching from a normal operating mode into a test mode dependent on and responsive to the result of evaluating this externally applied potential. To the contrary, both of the references involve only the application of a test-triggering signal via **input pins** provided for this purpose. Neither reference provides any suggestion or motivation toward applying such a test-trigger signal to the output pins (18) of Habersetzer et al., or (14 and 24) of Chai et al. Thus, the invention of present independent claim 21 and its dependent claims would not have been obvious over the prior art. The Examiner is respectfully requested to withdraw the rejection of claims 21 to 23 and 25 (and apparently also 29, 30, 33 and 34) as obvious over Habersetzer et al. in view of Chai et al.

10) Favorable reconsideration and allowance of the application, including all present claims 21 to 36, are respectfully requested.

Respectfully submitted,

Matthias EICHIN et al.
Applicant

By _____
Walter F. Fasse
Patent Attorney
Reg. No.: 36132
Tel. 207-862-4671
Fax. 207-862-4681
P. O. Box 726
Hampden, ME 04444-0726

WFF:ar/4284
Enclosures:
copy of return receipt
postcard of 04/21/03

CERTIFICATE OF FAX TRANSMISSION:

I hereby certify that this correspondence with all indicated enclosures is being transmitted by telefax to (703) 872-9306 on the date indicated below, and is addressed to: COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450.

_____ 12/9/04
Name: Walter F. Fasse - Date: December 9, 2004